Host Interface

- Supports 16-bit PC Card
- Supports Local Bus I/F for External Processor
- Supports General DMA

External Memory Interface

- Supports External Flash, Asynchronous/ Synchronous RAM and Slave Devices
- Up to 4M-byte of Address Space Per Chip-Select Output
- Up to 44-MHz Access for Asynchronous Devices

Medium Access Controller

- MCU core : 44MHz Embedded ARM7TDMI CPU
- 1KB Boot ROM
- 64KB Zero-Wait SRAM for Code
- 64KB SRAM for Data and Memory Buffer
- Hardware-Based MAC Access Protocol Management
- Delayed Acknowledgement (DEL-ACK) and Hardware-Generated Immediate Acknowledgement (IMM-ACK)
- Channel Probing and Dynamic Link Quality Control
- Dynamic Allocation of Transmit (TX) and Receive (RX) Memory Blocks
- Hardware-Based RX Frame Parsing
- Hardware-Based Encryption/Decryption using CCM(CTR+CBC-MAC) Mode that use the 128-bit AES as a Block Cipher Algorithm

Baseband Processor

- KOINONIA WPAN Spec. V.1.X & V2.0 Compliant
- Dual Chip-rate Support : 5.5 or 11M chip/sec
- Supports KOINONIA's Binary CDMA Transmission.
- Variable Data Rate :
  - 0.34375M, 1.03125M, 3.09375M, 6.1875M, 11M, 16.5M, 22M, 27.5M at 5.5M chip/sec
  - 0.6875M, 2.0625M, 6.1875M,12.375Mbps 22M, 33M, 44M, 55M at 11M chip/sec
- Multi-code Transmission
- Spreading Gain : 16, 16/3, 16/9
- CCA Detection
- Energy Level Detection
- RSSI Detection
- Multi-path Delay Spread Tolerance > 300ns

Radio Interface

- On-chip 10-bit, 44MHz Differential DACs for In-Phase and Quadrature TX Outputs
- On-chip 10-bit, 44MHz Differential ADCs for In-Phase and Quadrature RX Inputs
- Analog/Digital RX Automatic Gain Control (AGC) Outputs

System Level

- Single-Chip MAC and Baseband Processor
- 3-wire Serial EEPROM Interface
- 16C550 Compatible UART
- 32-bit Watch-dog Timer
- Four 32-bit Counters/Timers
- 32 GPIO Signals with Interrupt Capability
- Supports JTAG Boundary Scan
- 1.8V Low-Power Core Supply Voltage
- 3.3V I/O Supply Voltage
- 288-pin FBGA package
- On-chip PLL for 44MHz System Clock
- Low Power Mode

■ Description

The KWPAN1200 is a high performance single-chip medium-access controller (MAC) and baseband processor that is compliant with KOINONIA wireless personal area networks (WPAN) spec ver.1.0 / ver.1.1 / ver.2.0.

■ Applications

Typical applications for the KWPAN1200 include **:**

- High-speed low-cost WPAN access points (APs)
- 2.4-GHz wireless home-networking solution
- Wireless digital video recording (DVR) solution
- Devices with PC Card interface such as PDAs and digital cameras

Figure 1 shows a typical KWPAN1200 host-adapter system that features a 16-bit PC Card host interface, the KWPAN1200 chip with embedded CPU (ARM7TDMI), external memory and a 2.4GHz radio.

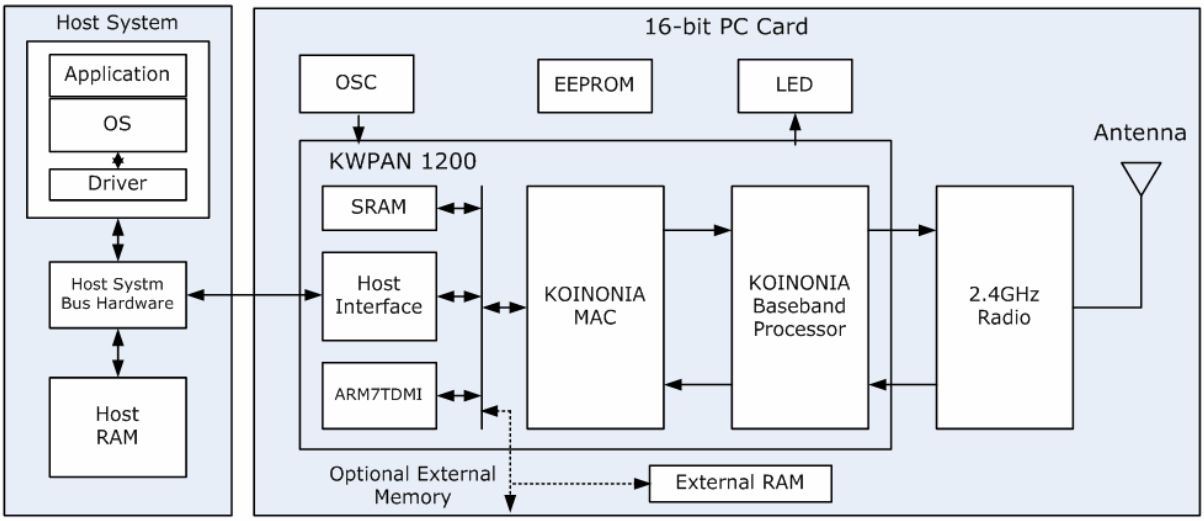


Figure 1. KWPAN1200 Adaptor Block Diagram

■ Package

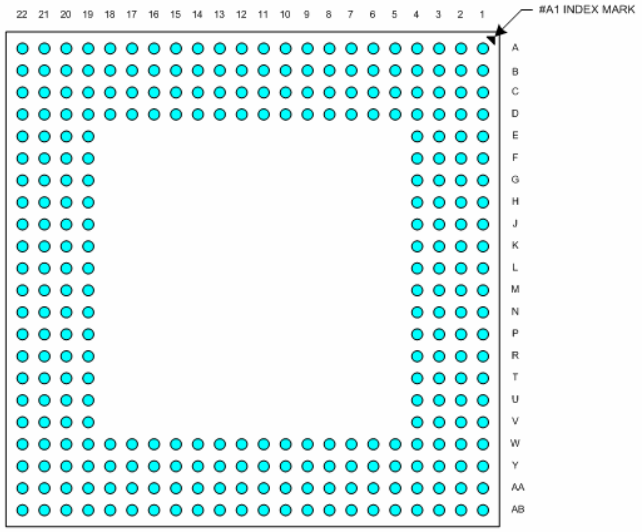


Figure 2. FBGA Package (Bottom View)

■ Functional Block Diagram

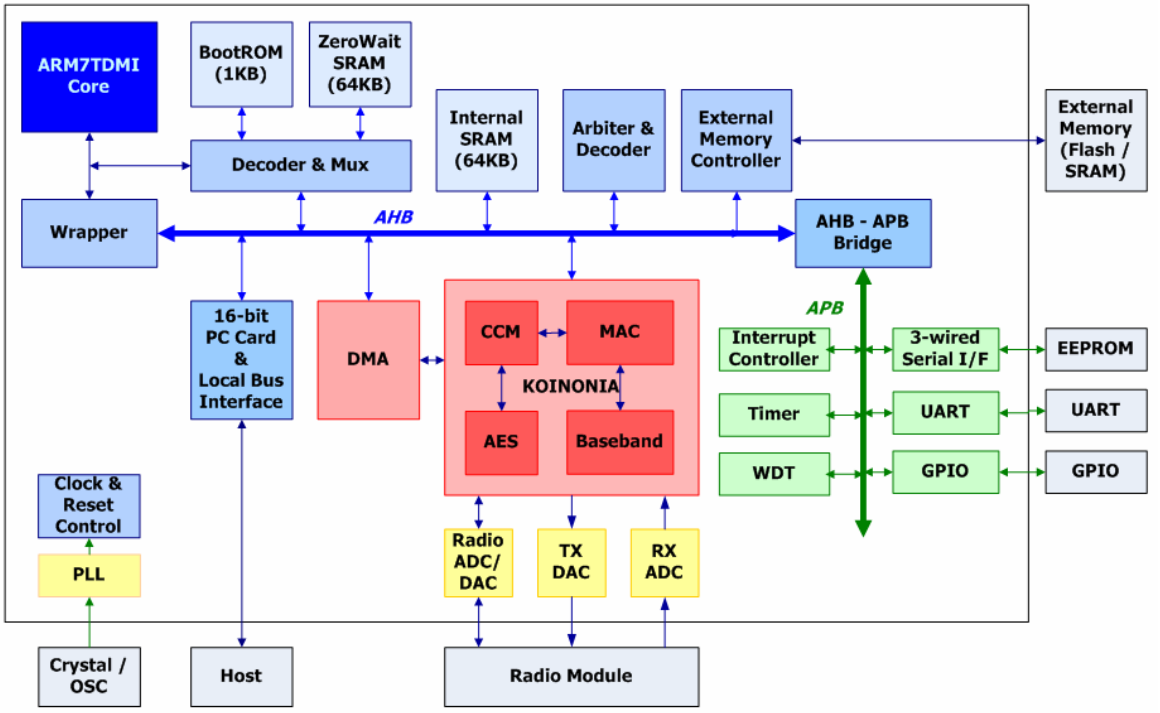


Figure 3. KWPAN1200 Functional Block Diagram

■ PIN Assignment

Table 1. Name-to-Number Mapping for 288 FBGA Package

NAME	No.	NAME	No.	NAME	No.
ADC_RXD_CML	G2	EDATA[0]	C14	GPIO[7]	Y14
ADC_RXD_REFBOT	G1	EDATA[1]	D14	GPIO[8]	AA14
ADC_RXD_REFTOP	E2	EDATA[2]	A14	GPIO[9]	AB15
ADC_RXI_N	E1	EDATA[3]	B13	GPIO[10]	Y15
ADC_RXI_P	F1	EDATA[4]	A13	GPIO[11]	AA15
ADC_RXQ_N	J1	EDATA[5]	C13	GPIO[12]	AB16
ADC_RXQ_P	H1	EDATA[6]	B12	GPIO[13]	Y16
ADC_SPEEDUP	F2	EDATA[7]	A12	GPIO[14]	AA16
AGC_B[0]	H2	EDATA[8]	C12	GPIO[15]	AB17
AGC_B[1]	J2	EDATA[9]	D12	GPIO[16]	Y17
AGC_B[2]	K2	EDATA[10]	B11	GPIO[17]	AA17
AGC_B[3]	L2	EDATA[11]	A11	GPIO[18]	AB18
AGC_B[4]	K1	EDATA[12]	C11	GPIO[19]	AA18
AGC_B[5]	L1	EDATA[13]	D11	GPIO[20]	AB19
AGC_B[6]	M2	EDATA[14]	B10	GPIO[21]	Y19
DAC_TXD_CCOMP	T1	EDATA[15]	A10	GPIO[22]	AA19
DAC_TXD_IRSET	T2	EDATA[16]	C10	GPIO[23]	AB20
DAC_TXD_SIN	U2	EDATA[17]	C9	GPIO[24]	AB21
DAC_TXD_VREF	R2	EDATA[18]	A9	GPIO[25]	AA21
DAC_TXI_N	U1	EDATA[19]	D9	GPIO[26]	AB22
DAC_TXI_P	V1	EDATA[20]	B9	GPIO[27]	W20
DAC_TXQ_N	R1	EDATA[21]	B8	GPIO[28]	AA22
DAC_TXQ_P	P1	EDATA[22]	A8	GPIO[29]	Y21
EADDR[0]	B21	EDATA[23]	C8	GPIO[30]	V20
EADDR[1]	C19	EDATA[24]	B7	GPIO[31]	Y22
EADDR[2]	A21	EDATA[25]	A7	HostAddr[0]	P21
EADDR[3]	B20	EDATA[26]	C7	HostAddr[1]	P20
EADDR[4]	D18	EDATA[27]	B6	HostAddr[2]	P22
EADDR[5]	A20	EDATA[28]	A6	HostAddr[3]	N19
EADDR[6]	B19	EDATA[29]	C6	HostAddr[4]	N21
EADDR[7]	C18	EDATA[30]	C5	HostAddr[5]	N20
EADDR[8]	A19	EDATA[31]	B5	HostAddr[6]	N22
EADDR[9]	B18	EFRPn	A1	HostAddr[7]	M19
EADDR[10]	D17	EFWPn	B2	HostAddr[8]	M20
EADDR[11]	A18	EMBEn[0]	A5	HostAddr[9]	M22
EADDR[12]	B17	EMBEn[1]	C4	HostAddr[10]	M21
EADDR[13]	C17	EMBEn[2]	B4	HostAddr[11]	L21
EADDR[14]	D16	EMBEn[3]	A4	HostAddr[12]	L19
EADDR[15]	A17	EMEMCLK	B14	HostAddr[13]	L22
EADDR[16]	B16	EOEn	A3	HostAddr[14]	L20
EADDR[17]	A16	EWEn	D4	HostAddr[15]	K21
EADDR[18]	C16	GPIO[0]	Y11	HostAddr[16]	K19
EADDR[19]	B15	GPIO[1]	Y12	HostAddr[17]	K22
EADDR[20]	A15	GPIO[2]	AA12	HostAddr[18]	K20
EADDR[21]	C15	GPIO[3]	AB13	HostAddr[19]	J21
ECS0n	C3	GPIO[4]	Y13	HostAddr[20]	J22
ECS1n	B3	GPIO[5]	AA13	HostAddr[21]	J20
ECS2n	A2	GPIO[6]	AB14	HostAddr[22]	J19

NAME	No.
HostCE1n	D19
HostCE2n	C21
HostData[0]	H21
HostData[1]	H22
HostData[2]	H20
HostData[3]	G21
HostData[4]	G22
HostData[5]	G20
HostData[6]	G19
HostData[7]	F21
HostData[8]	F20
HostData[9]	F20
HostData[10]	E21
HostData[11]	E22
HostData[12]	E20
HostData[13]	D21
HostData[14]	D22
HostData[15]	E19
HostIREQn	C20
HostOEn	C22
HostREGn	B22
HostWAITn	A22
HostWEn	D20
S3W_CS	R20
S3W_DIN	R22
S3W_DOUT	P19
S3W_SCK	R21
JTAG_nTRST	AA6
JTAG_TCK	AB4
JTAG_TDI	AB3
JTAG_TDO	AB5
JTAG_TMS	AA5
NRXTX	R19
PA_EN	W22
PLL_FILTER	AB9
POReseth	AA11
POResetn	AB12
RF_CSB	U22
RF_GAIN	V21
RF_SCLK	T21
RF_SDOUT	T20
RF_SHDNB	U21
RF_SHDNB2	T22
RX_1K	T19
RX_ON	V22
TEST_MODE[0]	AB2
TEST_MODE[1]	AA3
TEST_MODE[2]	Y4

NAME	No.
TEST_MODE[3]	AA4
TEST_MODE[4]	AB11
TEST_MODE[5]	AB10
TEST_MODE[6]	AA10
TR_SW	W21
TR_SWN	U19
TX_ON	U20
TX_RX_AGC_NBIAS	M1
TX_RX_AGC_VOUT	N2
TX_RX_AGC_VRB	P2
TX_RX_AGC_VRT	N1
UART_RXD	AA7
UART_RXD1	AA8
UART_TXD	AB6
UART_TXD1	AB7
XTAL_IN	AB8
XTAL_OUT	AA9
GND	B1
GND	C1
GND	C2
GND	D1
GND	D2
GND	D3
GND	D5
GND	D6
GND	E3
GND	E4
GND	H3
GND	J3
GND	J4
GND	K3
GND	K4
GND	L3
GND	T3
GND	U3
GND	U4
GND	V2
GND	V3
GND	V4
GND	W1
GND	W2
GND	W3
GND	W4
GND	W14
GND	W15
GND	W17
GND	W18
GND	W19

NAME	No.
GND	Y1
GND	Y2
GND	Y3
GND	Y5
GND	Y6
GND	Y7
GND	Y18
GND	Y20
GND	AA1
GND	AA2
GND	AA20
GND	AB21
GNDA	F4
GNDA	G4
GNDA	N4
GNDA	P4
GNDA	R4
GNDA	T4
GNDA	W10
GNDA	W11
VDD18	D7
VDD18	D10
VDD18	D15
VDD18	F19
VDD18	H4
VDD18	M4
VDD18	V19
VDD18	W5
VDD18	W6
VDD18	W8
VDD18	W13
VDD18	Y10
VDD18A	F3
VDD18A	G3
VDD18A	M3
VDD18A	N3
VDD18A	P3
VDD18A	R3
VDD18A	Y9
VDD33	D8
VDD33	D13
VDD33	H19
VDD33	L4
VDD33	W7
VDD33	W9
VDD33	W12
VDD33	W16
VDD33	Y8

■ PIN Assignment

Table 2. Number-to-Name Mapping for 288 FBGA Package

No.	NAME	No	NAME	No.	NAME
A1	EFRPn	C5	EDATA[30]	F1	ADC_RXI_P
A2	ECS2n	C6	EDATA[29]	F2	ADC_SPEEDUP
A3	EOEn	C7	EDATA[26]	F3	VDD18A
A4	EMBEn[3]	C8	EDATA[23]	F4	GNDA
A5	EMBEn[0]	C9	EDATA[17]	F19	VDD18
A6	EDATA[28]	C10	EDATA[16]	F20	HostData[9]
A7	EDATA[25]	C11	EDATA[12]	F21	HostData[7]
A8	EDATA[22]	C12	EDATA[8]	F22	HostData[8]
A9	EDATA[18]	C13	EDATA[5]	G1	ADC_RXD_REFBOT
A10	EDATA[15]	C14	EDATA[0]	G2	ADC_RXD_CML
A11	EDATA[11]	C15	EADDR[21]	G3	VDD18A
A12	EDATA[7]	C16	EADDR[18]	G4	GNDA
A13	EDATA[4]	C17	EADDR[13]	G19	HostData[6]
A14	EDATA[2]	C18	EADDR[7]	G20	HostData[5]
A15	EADDR[20]	C19	EADDR[1]	G21	HostData[3]
A16	EADDR[17]	C20	HostIREQn	G22	HostData[4]
A17	EADDR[15]	C21	HostCE2n	H1	ADC_RXQ_P
A18	EADDR[11]	C22	HostOEn	H2	AGC_B[0]
A19	EADDR[8]	D1	GND	H3	GND
A20	EADDR[5]	D2	GND	H4	VDD18
A21	EADDR[2]	D3	GND	H19	VDD33
A22	HostWAITn	D4	EWEn	H20	HostData[2]
B1	GND	D5	GND	H21	HostData[0]
B2	EFWPn	D6	GND	H22	HostData[1]
B3	ECS1n	D7	VDD18	J1	ADC_RXQ_N
B4	EMBEn[2]	D8	VDD33	J2	AGC_B[1]
B5	EDATA[31]	D9	EDATA[19]	J3	GND
B6	EDATA[27]	D10	VDD18	J4	GND
B7	EDATA[24]	D11	EDATA[13]	J19	HostAddr[22]
B8	EDATA[21]	D12	EDATA[9]	J20	HostAddr[21]
B9	EDATA[20]	D13	VDD33	J21	HostAddr[19]
B10	EDATA[14]	D14	EDATA[1]	J22	HostAddr[20]
B11	EDATA[10]	D15	VDD18	K1	AGC_B[4]
B12	EDATA[6]	D16	EADDR[14]	K2	AGC_B[2]
B13	EDATA[3]	D17	EADDR[10]	K3	GND
B14	EMEMCLK	D18	EADDR[4]	K4	GND
B15	EADDR[19]	D19	HostCE1n	K19	HostAddr[16]
B16	EADDR[16]	D20	HostWEn	K20	HostAddr[18]
B17	EADDR[12]	D21	HostData[13]	K21	HostAddr[15]
B18	EADDR[9]	D22	HostData[14]	K22	HostAddr[17]
B19	EADDR[6]	E1	ADC_RXI_N	L1	AGC_B[5]
B20	EADDR[3]	E2	ADC_RXD_REFTOP	L2	AGC_B[3]
B21	EADDR[0]	E3	GND	L3	GND
B22	HostREGn	E4	GND	L4	VDD33
C1	GND	E19	HostData[15]	L19	HostAddr[12]
C2	GND	E20	HostData[12]	L20	HostAddr[14]
C3	ECS0n	E21	HostData[10]	L21	HostAddr[11]
C4	EMBEn[1]	E22	HostData[11]	L22	HostAddr[13]

No.	NAME
M1	TX_RX_AGC_NBIAS
M2	AGC_B[6]
M3	VDD18A
M4	VDD18
M19	HostAddr[7]
M20	HostAddr[8]
M21	HostAddr[10]
M22	HostAddr[9]
N1	TX_RX_AGC_VRT
N2	TX_RX_AGC_VOUT
N3	VDD18A
N4	GNDA
N19	HostAddr[3]
N20	HostAddr[5]
N21	HostAddr[4]
N22	HostAddr[6]
P1	DAC_TXQ_P
P2	TX_RX_AGC_VRB
P3	VDD18A
P4	GNDA
P19	S3W_DOUT
P20	HostAddr[1]
P21	HostAddr[0]
P22	HostAddr[2]
R1	DAC_TXQ_N
R2	DAC_TXD_VREF
R3	VDD18A
R4	GNDA
R19	NRXTX
R20	S3W_CS
R21	S3W_SCK
R22	S3W_DIN
T1	DAC_TXD_CCOMP
T2	DAC_TXD_IRSET
T3	GND
T4	GNDA
T19	RX_1K
T20	RF_SDOUT
T21	RF_SCLK
T22	RF_SHDNB2
U1	DAC_TXI_N
U2	DAC_TXD_SIN
U3	GND
U4	GND
U19	TR_SWN
U20	TX_ON
U21	RF_SHDNB
U22	RF_CSB

No	NAME
V1	DAC_TXI_P
V2	GND
V3	GND
V4	GND
V19	VDD18
V20	GPIO[30]
V21	RF_GAIN
V22	RX_ON
W1	GND
W2	GND
W3	GND
W4	GND
W5	VDD18
W6	VDD18
W7	VDD33
W8	VDD18
W9	VDD33
W10	GNDA
W11	GNDA
W12	VDD33
W13	VDD18
W14	GND
W15	GND
W16	VDD33
W17	GND
W18	GND
W19	GND
W20	GPIO[27]
W21	TR_SW
W22	PA_EN
Y1	GND
Y2	GND
Y3	GND
Y4	TEST_MODE[2]
Y5	GND
Y6	GND
Y7	GND
Y8	VDD33
Y9	VDD18A
Y10	VDD18
Y11	GPIO[0]
Y12	GPIO[1]
Y13	GPIO[4]
Y14	GPIO[7]
Y15	GPIO[10]
Y16	GPIO[13]
Y17	GPIO[16]
Y18	GND

No.	NAME
Y19	GPIO[21]
Y20	GND
Y21	GPIO[29]
Y22	GPIO[31]
AA1	GND
AA2	GND
AA3	TEST_MODE[1]
AA4	TEST_MODE[3]
AA5	JTAG_TMS
AA6	JTAG_nTRST
AA7	UART_RXD
AA8	UART_RXD1
AA9	XTAL_OUT
AA10	TEST_MODE[6]
AA11	POReseth
AA12	GPIO[2]
AA13	GPIO[5]
AA14	GPIO[8]
AA15	GPIO[11]
AA16	GPIO[14]
AA17	GPIO[17]
AA18	GPIO[19]
AA19	GPIO[22]
AA20	GND
AA21	GPIO[25]
AA22	GPIO[28]
AB1	GND
AB2	TEST_MODE[0]
AB3	JTAG_TDI
AB4	JTAG_TCK
AB5	JTAG_TDO
AB6	UART_TXD
AB7	UART_TXD1
AB8	XTAL_IN
AB9	PLL_FILTER
AB10	TEST_MODE[5]
AB11	TEST_MODE[4]
AB12	POResetn
AB13	GPIO[3]
AB14	GPIO[6]
AB15	GPIO[9]
AB16	GPIO[12]
AB17	GPIO[15]
AB18	GPIO[18]
AB19	GPIO[20]
AB20	GPIO[23]
AB21	GPIO[24]
AB22	GPIO[26]

■ PIN Descriptions

1. Reset and System Clock

Name	No.	I/O	Description	Internal Resistor
POResetn*	AB12	SI	System reset. Asserting Reset results the entire KWPAN1200 system to a known state. This signal is active low.	Pull up
POReseth*	AA11	SI	System reset. Asserting Reset results the entire KWPAN1200 system to a known state. This signal is active high.	Pull down
XTAL_IN	AB8	I	Output of a crystal or oscillator unit.	-
XTAL_OUT**	AA9	O	Output of a crystal unit XTAL_OUT = $\overline{XTAL\_IN}$.	-

SI : Schmitt trigger input, I: input, O: output
* To make a simple circuit, you can use either POResetn or POReseth.
** XTAL_OUT is connected using a 2~4 lead crystal unit.

2. PLL Interface

Name	No.	I/O	Description	Internal Resistor
PLL_FILTER	AB9	O	The external loop filter capacitor should be connected between the pin and AGND (1200pF).	

O : Output

3. Dedicated-test Interface (include JTAG and Test Port)

JTAG Interface

Name	No.	I/O	Description	Internal Resistor
JTAG_TDI	AB3	SI	Test data in. TDI is used to serially shift test data and instructions into the KWPAN10A.	pull-up
JTAG_TMS	AA5	SI	Test mode select. TMS provides a means to control the state of the test access port (TAP) controller.	pull-up
JTAG_TCK	AB4	I	Test clock. TCK clocks serial test data and state information in and out of the KWPAN1200 on theTDI and TDO lines, respectively.	-
JTAG_TDO	AB5	O	Test data out. TDO is used to serialy shift test and instructions out of the KWPAN1200 .	-
JTAG_nTRST	AA6	SI	Test mode Reset.	pull-up

SI: Schmitt trigger input, I : input, O: output

Test Interface

Name	No.	I/O	Description	Internal Resistor
TEST_MODE [0:3]	AB2, AA3, Y4, AA4	SI	Test pin (normally, open).	pull-up
TEST_MODE [4:6]	AB11, AB10, AA10	I	Test pin (normally, Pull-down)	-

SI : Schmitt trigger input

4. Host Interface*

Name	No.	I/O	Description	Internal Resistor
HostAddr [0:22]	P21, P20, P22, N19, N21 , N20, N22, M19, M20, M22, M21, L21, L19, L22, L20, K21, K19, K22, K20, J21, J22, J20, J19	3SIO	these signals provide a 23-bit input host address bus.	Input : pull-up Output : Tri-State
HostData [0:15]	H21, H22, H20, G21, G22, G20, G19, F21, F22, F20, E21, E22, E20, D21, D22, E19	3SIO	In Normal Mode, these signals provide a 16-bit bidirectional data bus. In 32-bit External Memory Interface (EMI) Mode, these signals provide the high 16 bits of the 32-bit external memory data bus.	Input : pull-up Output : Tri-State
HostWEn†	D20	SI	Write Enable.	pull-up
HostOEn†	C22	SI	Output Enable.	pull-up
HostCE1n†	D19	SI	Chip Select 1.	pull-up
HostCE2n†	C21	SI	Chip Select 2.	pull-up
HostIREQn†	C20	O	In Normal Mode, it is IREQ. In 32-bit EMI Mode, it is 3th_Byte_Enable.	-
HostWAITn†	A22	O	In Normal Mode, it is WAIT. In 32-bit EMI Mode, it is 4th_Btye_Enable.	-
HostREGn†	B22	SI	Indicate Attribute Memory Access.	pull-up

3IO : 3-state Bidirectional Input/Output, 3SIO : Schmitt Trigger, SI : Schmitt trigger input, O : Output
* Host Interface can support only 16-bit access.
† This is an active-low signal.

5. External Memory Interface

Name	No.	I/O	Description	Internal Resistor
EADDR[0:21]	B21, C19, A21, B20, D18, A20, B19, C18, A19, B18, D17, A18, B17, C17, D16, A17, B16, A16, C16, B15, A15, C15	O	22-bit External Memory address.	-
EMEMCLK	B14	O	External Memory Clock is a system-clock-out signal.	-
EDATA[0:31]	C14, D14, A14, B13, A13, C13, B12, A12, C12, D12, B11, A11, C11, D11, B10, A10, C10, C9, A9, D9, B9, B8, A8, C8, B7, A7, C7, B6, A6, C6, C5, B5	3IO	External Memory Data bus or KWPAN1200 configuration.	none
EMBEn[0:3]†	A5, C4, B4, A4	O	External Memory Byte Enable.	-
ECS0n†	C3	O	External Memory Chip Select 0.	-
ECS1n†	B3	O	External Memory Chip Select 1.	-
ECS2n†	A2	O	External Memory Chip Select 2.	-
EOEn†	A3	O	External Memory Output Enable.	-
EWEn†	D4	O	External Memory Write Enable.	-
EFWPn†	B2	O	External Flash Write Protect.	-
EFRPn†	A1	O	External Flash Reset and Deep Power Down.	-

O: Output, 3IO: 3-state Bidirectional Input/Output
† This is an active-low signal.

6. 3-wire Serial EEPROM Interface

Name	No.	I/O	Description	Internal Resistor
S3W_SCK	R21	O	3-wire serial interface Clock.	-
S3W_CS	R20	O	3-wire serial interface Chip Select.	-
S3W_DIN	R22	O	3-wire serial interface Data In.	-
S3W_DOUT	P19	I	3-wire serial interface Data Out.	-

O: Output, I: Input

7. General Purpose I/O

Name	No.	I/O	Description	Internal Resistor
GPIO [0 : 31]	Y11, Y12, AA12, AB13, AB14, Y14, AA14, AB15, AB16, Y11, Y12, AA12, AB13, AB14, Y14, AA14, AB15, AB16, Y16, AA16, AB17, Y17, AA17, AB18, AA18, AB19, Y19, AA19, AB20, AB21, AA21, AB22, W20, AA22, Y21, Y22	3IO	32-bit General-purpose I/O. The ARM7TDMI controls the functionality of these signals.	INPUT : Pull-up OUTPUT : Tri-State

3IO : 3-State Bidirectional Input/Output

8. UART Interface

Name	No.	I/O	Description	Internal Resistor
UART_TXD	AB6	O	transmitter output to External UART transceiver.	-
UART_RXD	AA7	I	receiver input from External UART transceiver.	-
UART_TXD1	AB7	O	transmitter output to External UART transceiver.	-
UART_RXD1	AA8	I	receiver input from External UART transceiver.	-

O: Output, I : Input

9. Radio Interface

Name	No.	I/O	Description	Internal Resistor
TR_SW	W21	O	TR_SW changes state from receiving state to transmitting state or from transmitting state to receiving state in front of antenna. This is a complement for TR_SWN(pin R15) for differential drive of Tx/Rx switches.	-
TR_SWN	U19	O	TR_SWN changes state from receiving state to transmitting state or from transmitting state to receiving state in front of antenna. This is a complement for TR_SW(pin U14) for differential drive of Tx/Rx switches.	-
PA_EN	W22	O	Power amplifier enable output. The MCU controls the polarity of this signal.	-
RF_GAIN	V21	O	RF LNA gain control output. KWPAN1200 asserts this signal to switch on/off the RF LNA.	-
TX_ON	U20	O	TX_ON control output.	-
RX_ON	V22	O	RX_ON control output.	-
RX_1K	T19	O	Receiver 1KHz Highpass Bandwidth control output. The MCU controls the polarity of this signal.	-
RF_SHDNB	U21	O	RF chip Shutdown control output. The MCU controls the polarity of this signal.	-
RF_SHDNB2	T22	O	RF chip Shutdown control output for MAX2831 RF chipset.	-
NRXTX	R19	O	RX/TX Mode Control Logic Output for MAX2831 RF chipset. See Table for operating modes.	-
RF_CSB	U22	O	Serial data enable output. RF_CSB is active low.	-
RF_SCLK	T21	O	Serial clock output. RF_SCLK latches data on RF_SDOUT to the RF module. Data is latched on the rising edge of RF_SCLK.	-
RF_SDOUT	T20	O	Serial data output. RF_SDOUT carries serial data that is latched to the radio on the rising edge of RF_SCLK. The KWPAN1200 provides this data in the 6 Word (16bit) registers.	-
AGC_B[0:6]	H2,J2,K2,L2,K1,L1,M2	O	RX/TX Gain-Control Digital Output Bit[0~6]	

O : Output

RF Mode	Logic Ouptput				
	RF_SHDNB	TX_ON	RX_ON	RF_SHDNB2	NRXTX
Shut down	0	0	0	0	0
Stanby	1	0	0	0	1
RX	1	0	1	1	0
TX	1	1	0	1	1

10. TX DATA DAC (I&Q Channel) – refer to Figure 4

Name	No.	I/O	Description	Internal Resistor
DAC_TXI_P	V1	AO(1.8V)	Transmit In-Phase Positive	-
DAC_TXI_N	U1	AO(1.8V)	Transmit In-Phase Negative	-
DAC_TXQ_P	P1	AO(1.8V)	Transmit Quadrature Positive.	-
DAC_TXQ_N	R1	AO(1.8V)	Transmit Quadrature Negative.	-
DAC_TXD_CCOMP	T1	AO(1.8V)	Using Compensation Capacitor (0.1uF).	-
DAC_TXD_SIN	U2	AO(1.8V)	Using Compensation Capacitor (0.1uF).	-
DAC_TXD_VREF	R2	AI(1.8V)	Reference Input Voltage (0.4V).	-
DAC_TXD_IRSET	T2	AI(1.8V)	External Resistor for Current Setting (1.27K).	-

AI : Analog input, AO : analog output

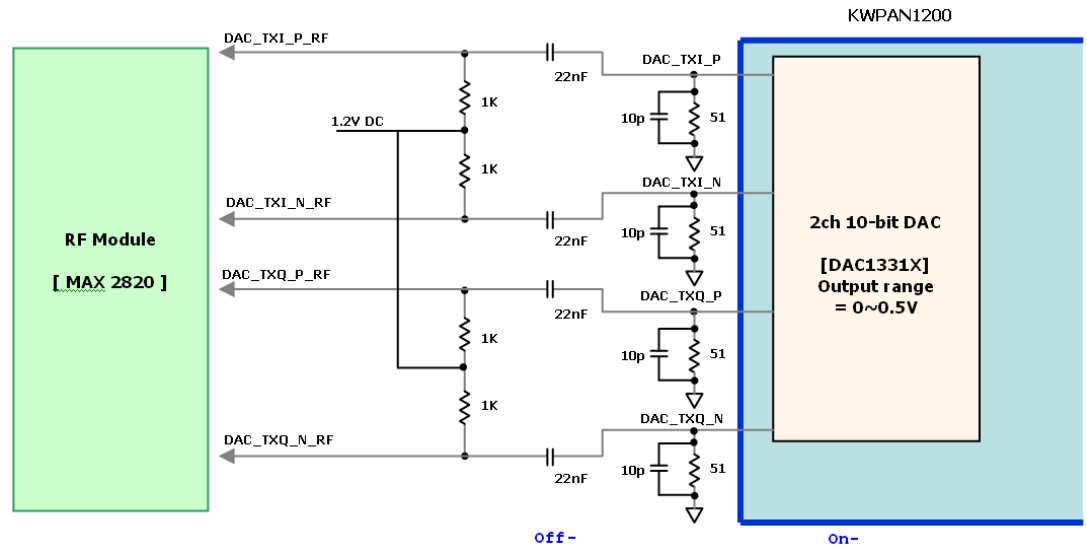


Figure 4. TX DATA DAC Interface Circuit Example

11. TX & RX AGC DAC - Direct Connection to RF TX_RX AGC Pin

Name	No.	I/O	Description	Internal Resistor
TX_RX_AGC_VRT	N1	AI(1.8V)	TX AGC Voltage Reference Top (1.8V).	
TX_ RX_AGC_VRB	P2	AI(1.8V)	TX AGC Voltage Reference Bottom (0V).	
TX_ RX_AGC_NBIAS	M1	AO(1.8V)	TX AGC Bias Generator Output (Normally,Open).	
TX_ RX_AGC_VOUT	N2	AO(1.8V)	TX AGC Analog Voltage Output.	
AGC_B[0:6]	H2, J2, K2, L2, K1, L1, M2	O	TX AGC Voltage Reference Top (1.8V).	

AI : Analog input, AO : analog output, O : output

12. Rx DATA ADC (I&Q Channel) – refer to figure 5

Name	No.	I/O	Description	Internal Resistor
ADC_RXI_P	F1	AI (1.8V)	Receive In-Phase Positive.	(50ohm)
ADC_RXI_N	E1	AI (1.8V)	Receive In-Phase Negative.	(50ohm)
ADC_RXQ_P	H1	AI (1.8V)	Receive Quadrature Positive.	(50ohm)
ADC_RXQ_N	J1	AI (1.8V)	Receive Quadrature Negative.	(50ohm)
ADC_RXD_CML	G2	AI(1,8V)	Test Pin (normally, open).	
ADC_SPEEDUP	F2	AI(1,8V)	Speed Test pin (Normally, AVDD18A).	
ADC_RXD_REFTOP	E2	AI(1,8V)	1.15V Internal Reference Top Voltage (normally, Open).	
ADC_RXD_REFBOT	G1	AI(1,8V)	0.65V Internal Reference Bottom Voltage (normally, Open).	

AI : Analog input, AO : analog output

- ADC_RXI_P, ADC_RXI_N, ADC_RXQ_P, ADC_RXQ_N input nodes are internally self-biased as the VDD18A/2 voltages. Input impedance through the power supply is 3K Ohm and the impedance between input nodes is 2K Ohm

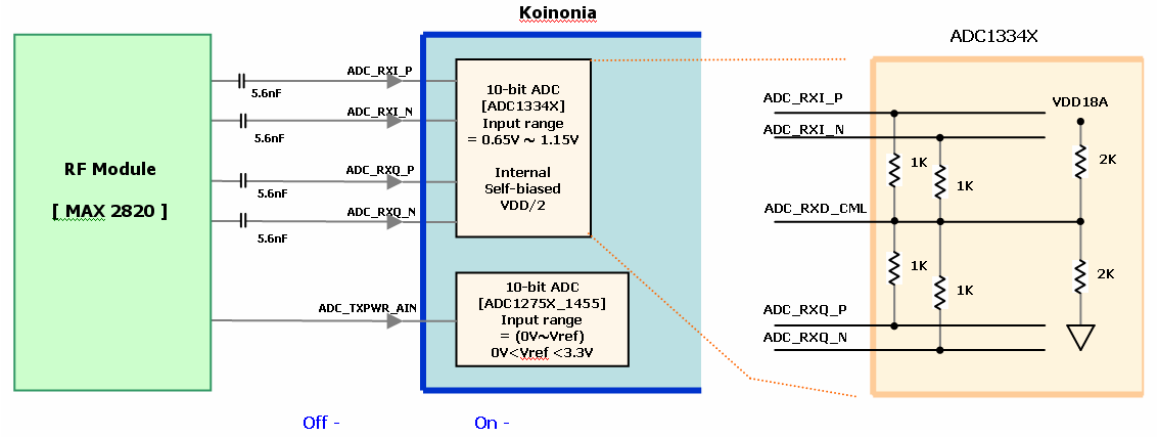


Figure 5. Rx DATA ADC Interface Circuit Example.

13. KWPAN1200 I/O Pins to RF Chipset pins Mapping Table

	RATE / KWPAN1200	RATE1~RATE4		RATE1~RATE8	
		MAX2820 MAX2821	MAX2822	MAX2829	MAX2831
Tx Data	DAC_TXI_P	TX_BBIP	TX_BBIP	TXBBI+	TXBBI+
	DAC_TXI_N	TX_BBIN	TX_BBIN	TXBBI-	TXBBI-
	DAC_TXQ_P	TX_BBQP	TX_BBQP	TXBBQ+	TXBBQ+
	DAC_TXQ_N	TX_BBQN	TX_BBQN	TXBBQ-	TXBBQ-
Rx Data	ADC_RXI_P	RX_BBIP	RX_BBIP	RXBBI+	RXBBI+
	ADC_RXI_N	RX_BBIN	RX_BBIN	RXBBI-	RXBBI-
	ADC_RXQ_P	RX_BBQP	RX_BBQP	RXBBQ+	RXBBQ+
	ADC_RXQ_N	RX_BBQN	RX_BBQN	RXBBQ-	RXBBQ-
AGC	TX_ RX_AGC_VOUT	TX_GC RX_AGC	TX_GC RX_AGC	NC	NC
	AGC_B0	NC	NC	B1	B1
	AGC_B1	NC	NC	B2	B2
	AGC_B2	NC	NC	B3	B3
	AGC_B3	NC	NC	B4	B4
	AGC_B4	NC	NC	B5	B5
	AGC_B5	NC	NC	B6	B6
	AGC_B6	NC	NC	B7	B7
TX/RX Enable	TX_ON	TX_ON	TX_ON	TXENA	NC
	RX_ON	RX_ON	RX_ON	RXENA	NC
	NRXTX	NC	NC	NC	RXTX
LNA	RF_GAIN	RF_GAIN	RF_GAIN	NC	NC
Filter	RX_1K	RX_1K	RX_1K	RX_HP	RXHP
Shutdown	RF_SHDNB	SHDNB	SHDNB	SHDNB	NC
	RF_SHDNB2	NC	NC	NC	SHDNB
3-Wire	RF_CSB	CSB	CSB	CSB	CSB
	RF_SCLK	SCLK	SCLK	SCLK	SCLK
	RF_SDOUT	DIN	DIN	DIN	DIN
PA	PA_EN	External PA	NC	External PA	NC
Switch	TR_SW	External S/W	NC	External S/W	External S/W
	TR_SWN	External S/W	NC	External S/W	External S/W

- The MAX2820 and MAX2821single-chip zero-IF transceivers are designed for the 802.11b (11Mbps) applications operating in the 2.4GHz to 2.5GHz ISM band.
- The MAX2822 single-chip transceiver is designed for 802.11b (11Mbps) applications operating in the 2.4GHz to 2.5GHz ISM band. The transceiver includes all the circuitry required to implement an 802.11b RF-to-baseband transceiver solution, including the power amplifier,transmit/receive switch, and 50 Ohm matching.
- The MAX2829 single-chip, RF transceiver ICs are designed specifically for OFDM 802.11 WLAN application. The MAX2829 is designed for dual-band 802.11a/g applications covering world-bands of 2.4GHz to 2.5GHz and 4.9GHz to 5.875GHz
- The MAX2831 direct conversion, zero-IF, RF transceiver is designed specifically for 2.4GHz to 2.5GHz 802.11g/b WLAN applications. The MAX2831 completely integrates all circuitry recuired to implement the RF transceiver function, providing an RF power amplifier(PA),RF-to-baseband receive path,baseband-to-RF transmit path, VCO,frequency synthesizer,crystal oscillator, and baseband/control interface.

14. Power & Ground

Name	No.	I/O	Description	Internal Resistor
GND	B1, C1, C2, D1, D2, D3, D5, D6, E3, D4, H3, J3, J4, K3, K4, L3, T3, U3, U4, V2, V3, V4, W1, W2, W3, W4, W14, W15, W17, W18, W19, Y1, Y2, Y3, Y5, Y6, Y7, Y18, Y20, AA1, AA2, AA20, AB1	G	Digital Ground	-
GNDA	F4, G4, N4, P4, R4, T4, W10, W11	G	Analog Ground	-
VDD18	D7, D10, D15, F19, H4, M4, V18, W5, W6, W8, W13, Y10	P	1.8V Digital Voltage Supply	-
VDD18A	F3, G3, M3, N3, P3, R3, Y9	P	1.8V Analog Voltage Supply	-
VDD33	D8, D13, H19, L4, W7, W9, W12, W16, Y8	P	3.3V Digital Voltage Supply	-

P : Power , G : ground

■ Sense-on-Reset Options

Name	Description
EDATA[0]	Enable Internal ROM. '0' : Disable internal ROM. '1' : Enable internal ROM, Only valid for Host_Interface_Type=2'b00.
EDATA[1]	Host Interface Type : EDATA[2:1]. "00" : Host Interface type is PC Card. "01" : Host Interface type is Stand Alone. "10" : Host Interface type is Local Bus of external processor. "11" : Test Mode.
EDATA[2]	
EDATA[3]	ECS0 Data Width : EDATA[4:3]. "00" : byte(8bit). "01" : half-word(16bit). "10" : word(32bit), Only valid for EDW = 1'b1 "11" : reserved.
EDATA[4]	
EDATA[5]	Reserved
EDATA[6]	PLL Control. '0' : PLL FOUT = XTAL_IN * 2. '1' : PLL FOUT = XTAL_IN * 4.
EDATA[7]	PLL Enable. '0' : PLL Disable. '1' : PLL Enable.
EDATA[8]	Reserved
EDATA[9]	System Clock. '0' : 22MHz. '1' : 44MHz.
EDATA[10]	Modem Test Mode. '0' : Normal. '1' : HostData is used for TestKoinData[15:0] and HostAddr[15:0] for TestKoinData[31:16].
EDATA[11]	System Test Mode. '0' : Normal. '1' : GPIO[7:0] is used for TestSystemData.
EDATA[12]	Reserved
EDATA[13]	Reserved
EDATA[14]	Reserved
EDATA[15]	Reserved

Note : Sense-on-Reset values are loaded during power-on and then system is configured according to ones.

■ Functional Description

◆ MAC

The KWPAN1200 implements the KOINONIA version 1.1 MAC sub-layer using both dedicated hardware and embedded firmware. The KOINONIA version 1.1 MAC functionality is partitioned between the host and the KWPAN1200 . KOINONIA version 1.1 MAC data service is provided by the MAC of the KWPAN1200 , while the host software, with the aid of the KWPAN1200 MAC, controls transmit and receive queue processing. The MAC hardware implements read-time functions, including access protocol management such as TDMA(Time Division Multiple Access) and CSMA/CA(Carrier Sense Multiple Access / Collision Avoidance) method, and direct memory access(DMA) transferring of data between the baseband processor and the internal RAM. The MCU(ARM7TDMI) runs firmware that manages the flow of commands and data to/from the host, performs scan-and-join operations, and maintains TX and RX queues. The MCU(ARM7TDMI) can override many of the MAC functions that are performed automatically by hardware during normal operation.
Figure 6 shows a block diagram of the MAC that includes the major functions and interfaces.

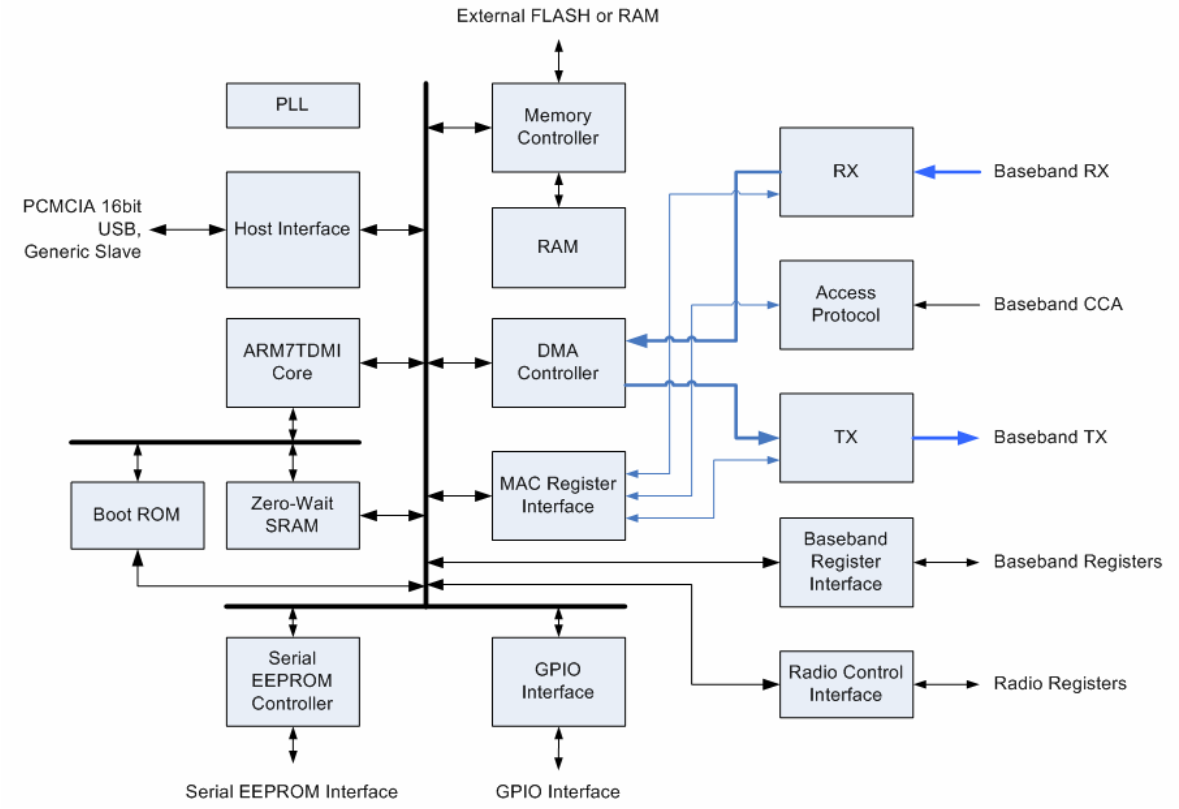


Figure 6. MAC Block Diagram

◆ MAC Interfaces

Host Interface

The KWPAN1200 host interface is defined as the slave to connect the KWPAN1200 to an external host. The host can transfer data to/from host memory, either directly or through a set of KWPAN1200 registers. The host interface provides the host with a set of commands that the host can configure, control, and use to obtain information from the KWPAN1200 . The host can optionally download code to KWPAN1200 memory over the host interface. There are two parallel host interface modes (PC Card, Generic Slave).

External-memory interface

The KWPAN1200 external-memory interface supports applications that require external flash, additional RAM. The MCU(ARM7TDMI) can obtain its code from either external flash or from the host. In either case, the code is copied to, and executed from, internal RAM to maximize throughput and minimize power.
Figure 7 shows an example external memory configuration that includes synchronous SRAM and flash devices.

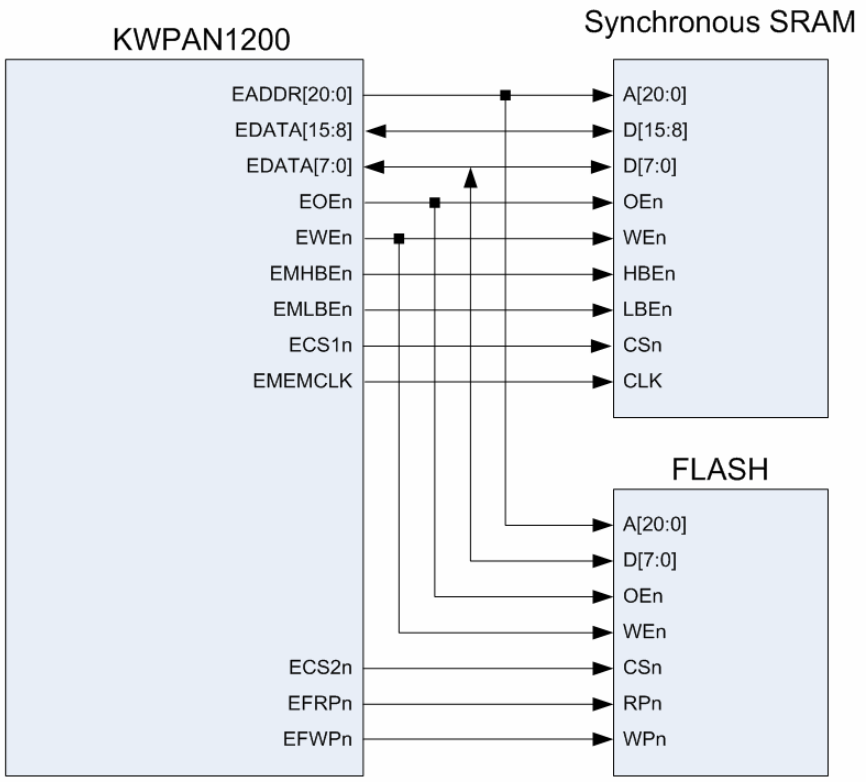


Figure 7. External Memory Interface Example

3-wire Serial EEPROM Interface

The EEPROM interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) supports standard 3-wire serial EEPROM devices that can provide nonvolatile storage for configuration parameters, such as the station's MAC address, PC Card configuration parameters, etc.
After setting HOST TYPE PC Card and powering up, almost of the contents in the EEPROM are read automatically and written to the appropriate KWPAN1200 registers or memory locations. The MCU(ARM7TDMI) and the host can read/write serial EEPROM through this interface.

Radio Control Interface

The radio control interface allows the KWPAN1200 to write control registers in some radio devices.

GPIO

The KWPAN1200 provides 32 programmable GPIO signals. The KWPAN1200 can configure the functionality of these signals.

◆ MAC Data Structures

To maximize internal memory utilization, the KWPAN1200 implements TX and RX data buffers using a linked list of memory blocks. The contents of the memory blocks are defined and referenced during TX and RX operations by means of queued descriptors. The host configures the size and location of the memory blocks and the descriptor queues during KWPAN1200 initialization. Allocation and deallocation of memory blocks are MCU(ARM7TDMI) functions. Typically, the data buffers exist in internal RAM, but they can be expanded by adding external RAM.

TX

To transmit a frame, the host first writes the frame to a linked list of free memory blocks within the KWPAN1200 . It then triggers an interrupt to the MCU(ARM7TDMI) to inform the KWPAN1200 that there is a frame in KWPAN1200 memory that is ready to transmit. In response, the MCU(ARM7TDMI) updates a new TX descriptor to a TX queue in KWPAN1200 memory. The MAC hardware initiates transmission after the medium access protocols have been met. The master device transmits beacon frame when new superframe starts. Both master device and slave devices transmit command frames or short data frames in CSMA/CA period when medium is idle and backoff procedure completes. And a device transmit appropriate frame in Contention-Free period when slot is allocated to that device and that slot is Tx mode. For unicast frames on TX completion, the MAC hardware waits to receive and ACK frame from the target station. If no ACK frame(ACK times out) or an invalid frame is returned, embedded firmware retries the hardware automatically retries the frame until the frame exchange is successful (a valid ACK frame is received) or a retry limit is reached. At that point, the TX hardware interrupts the MCU(ARM7TDMI), and the TX status is returned to the host through the associated TX descriptor.

RX

When a frame is received from the baseband processor, the RX hardware writes the frame to a linked list of free memory blocks. After the frame is completely received, the RX hardware checks the filtering and CRC. If it passes filtering and CRC checking, then the KWPAN1200 hardware interrupts the MCU(ARM7TDMI) to set up a RX descriptor in the RX queue for that frame. Subsequently, the MCU(ARM7TDMI) instructs the host to move the frame from KWPAN1200 to host memory.

DMA

The KWPAN1200 uses DMA to transfer data between the baseband processor and the internal RAM.

To transmit a frame, embedded firmware sets TX configuration parameters such as MAC header, PLCP header, etc. And then embedded firmware sets TX DMA registers such as the pointer that points the location of the next frame to transmit and the length of the next frame to transmit. Then TX hardware instructs the TX DMA to start transmitting frame. If transmitting frame is completed successfully, TX hardware disables the TX DMA engine. If TX FIFO under-run is occurred, TX hardware interrupts the MCU(ARM7TDMI) to inform that error is occurred in TX DMA engine and resets the TX DAMA engine.

When a frame is received from the baseband processor, RX hardware reports the length of the receiving frame. At that point, RX DMA engine knows the position of the memory block where receiving frame shall be stored. RX DMA engine counts the number of the received frame. If receiving frame is completed successfully, then RX DMA engine updates the register that points the memory block where next receiving frame shall be stored and KWPAN1200 interrupts the MCU(ARM7TDMI) to inform that there is a received frame in KWPAN1000A memory. If RX FIFO overflow or RX memory block overflow is occurred, RX DMA engine halts the receiving procedure and retrieves the position of the memory block where next receiving frame shall be stored and KWPAN1200 instructs the MCU(ARM7TDMI) to inform that error is occurred in RX DMA engine.

◆ Baseband Processor

■ Transmitter

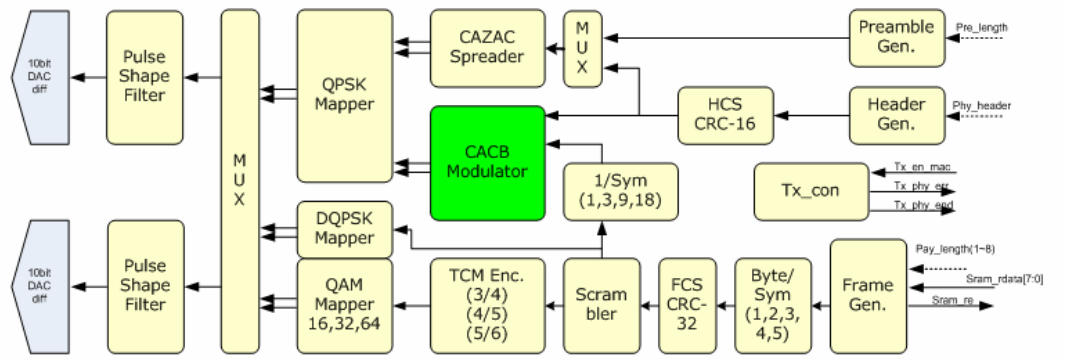


Figure 8. KOINONIA Baseband Processor, Transmitter Section

■ Receiver

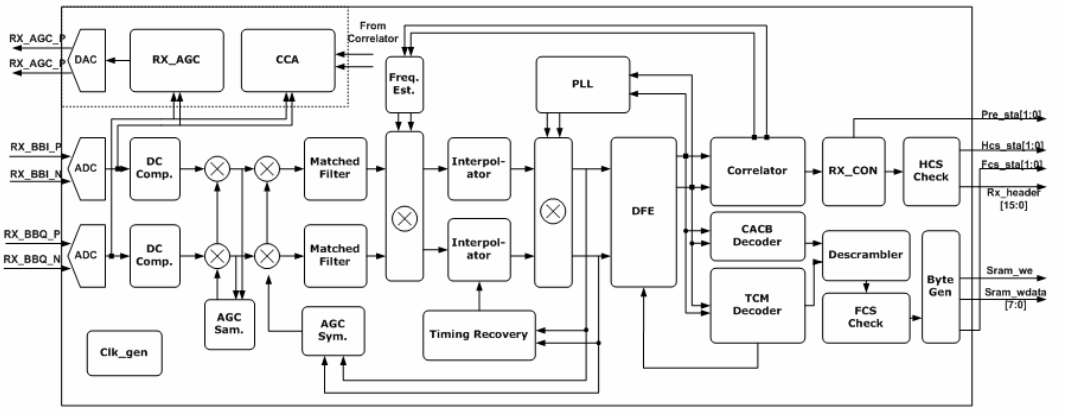


Figure 9. KONONIA Baseband Processor, Receiver Section

■ Electrical Specification

◆ DC Specification

■ Absolute Maximum Ratings

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	Vdd(1.8V)	2.7		V
	Vdd(3.3V)	4.8		
Input/Output Voltage	Vin/Vout(1.8V)	2.7		V
	Vin/Vout(3.3V)	4.8		
DC Input Current	Iin	+/- 200		mA
Storage Temperature	Tstg	PLASTIC	-65 to 150	°C

■ Recommended Operating Conditions

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	Vdd(1.8V)	1.65 to 1.95		V
	Vdd(3.3V)	3.0 to 3.6		
Input/Output Voltage	Vin/Vout(1.8V)	1.65 to 1.95		V
	Vin/Vout(3.3V)	3.0 to 3.6		
Operating Temperature	Topr (Commercial)	commercial	0 to 70	°C

■ DC Electrical Characteristics – Normal I/O (Vdd=1.65 to 1.95(V), Ta = 25(°C))

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Current	Iih	Vin=Vdd, Normal	-10	-	10	uA
Input Low Current	Iil	Vin=Vss, Normal	-10	-	10	uA

■ DC Electrical Characteristics – Normal I/O (Vdd=3.0 to 3.6(V), Ta = 25(°C))

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Current	Iih	Vin=Vdd, Normal	-10	-	10	uA
		Pull-Down , Down	10	-	60	uA
Input Low Current	Iil	Vin=Vss, Normal	-10	-	10	uA
		Pull-Up, Up	-60	-	-10	uA
Input High Voltage	Vih	CMOS	2.0	-	-	V
Input Low Voltage	Vil	CMOS	-	-	0.8	V
Output High Voltage	Voh	20mA Buffer, Ioh=- 20mA	2.4	-	-	V
		12mA Buffer, Ioh=- 12mA	2.4	-	-	V
		8mA Buffer, Ioh=- 8mA	2.4	-	-	V
		4mA Buffer, Ioh=- 4mA	2.4	-	-	V
Output Low Voltage	Vol	20mA Buffer, Iol= 20mA	-	-	0.4	V
		12mA Buffer, Iol= 12mA	-	-	0.4	V
		8mA Buffer, Iol= 8mA	-	-	0.4	V
		4mA Buffer, Iol= 4mA	-	-	0.4	V

■ Analog Front End

◆ RX DATA ADC (I&Q Channel)

Parameter	Min	Typ	Max	Unit
Analog Input voltage (+)	0.65	-	1.15	V
Analog Input voltage (-)	1.15	-	0.65	V
Internal Reference Input Voltage (TOP)	-	1.15	-	V
Internal Reference Input Voltage (BOT)	-	0.65	-	V
Input Impedance between input nodes	-	2	-	KΩ

◆ TX DATA DAC (I&Q Channel)

Parameter	Min	Typ	Max	Unit
Output voltage range (differential)	-	1	-	V_{PP}
Output Load Capacitor	-	10	-	pF
Output Load Resistor	-	50	-	Ω
Analog Output Settling Time	-	3.0	-	ns

◆ TX Power Sense ADC

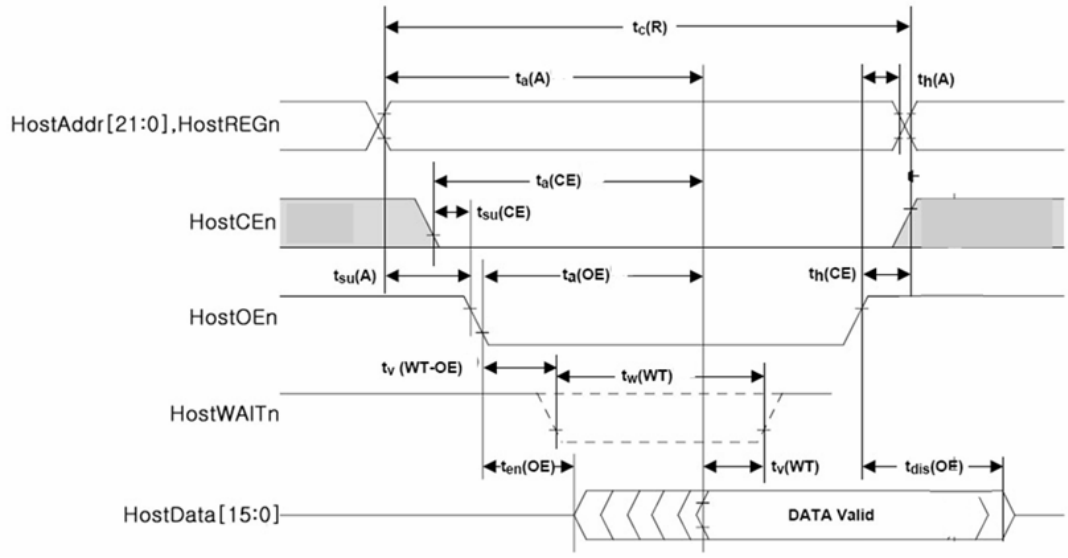
Parameter	Min	Typ	Max	Unit
Analog Input voltage	0	VREF	-	V
Internal Reference Input Voltage (VREF)	2.0	3.3	3.6	V
Internal Reference Input Voltage (GND)	0	0	0	V

◆ TX & Rx AGC DACs

Parameter	Min	Typ	Max	Unit
Supply Voltage (VDD - VSS)	1.7	1.8	1.9	V
Output voltage range	Vss	-	VDD	
Output Load Capacitor	-	-	20	pF
Output Load Resistor	100	-	-	KΩ
Analog Output Settling Time	-	100	-	ns

■ Host Interface (ref. IEEE)

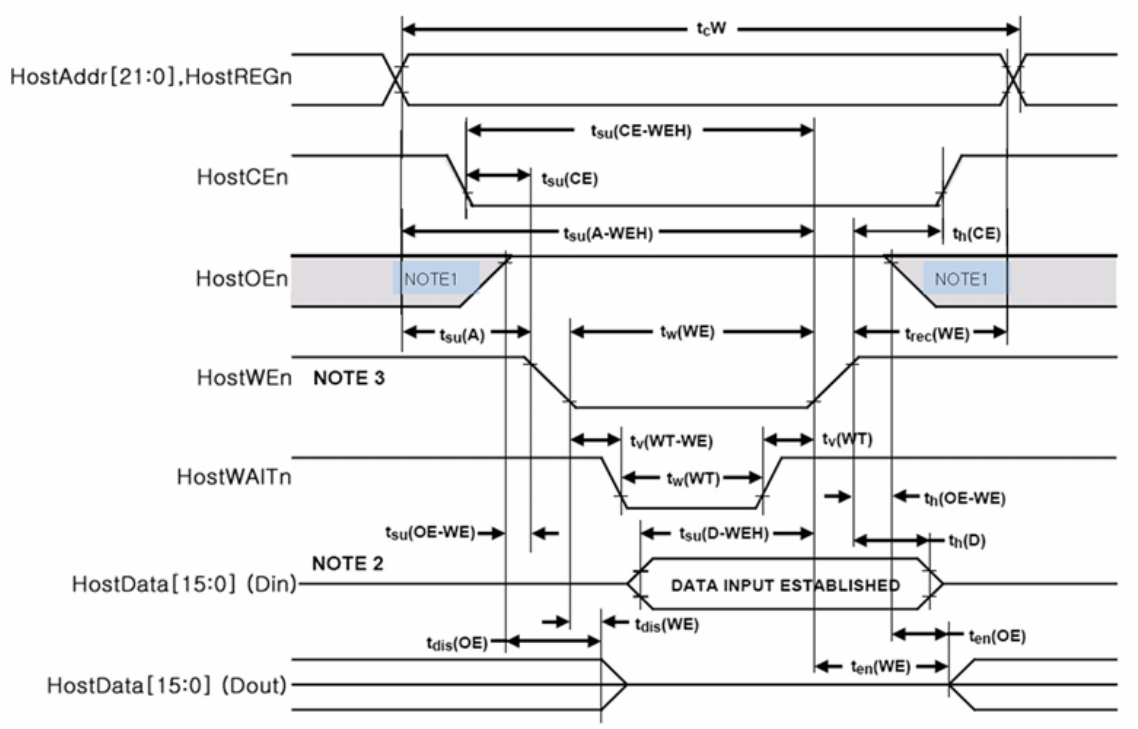
◆ Memory Read Timing Diagram



Speed Version			600 ns	
Item	Symbol	IEEEsymbol	Min(ns)	Max(ns)
Read cycle time	t_cR	tAVAV	600	
Address Access time	t_a(A)	tAVQV		600
Card Enable Access time	t_a(CE)	tELQV		600
Output Enable Access time	t_a (OE)	tGLQV		300
Output Disable Time from OEn(#)	t_{dis}(OE)	tGHQV		45
Output Enable Time from OEn	t_{en}(OE)	tGLQNZ	5	
Address Setup Time	t_{su}(A)	tAVGL	100	
Address Hold Time	t_h(A)	tGHAX	35	
Card Enable Setup Time	t_{su}(CE)	tELGL	0	
Card Enable Hold Time	t_h(CE)	tGHEH	35	
WAITn Valid from OEn	t_v(WT-OE)	tGLWTV		100
WAITn Pulse Width	t_w(WT)	tWTLWTH		12us
Data Setup for WAITn Released	t_v(WT)	tQVWTH	0	

* These timing are specified for hosts and PC card which support the HostWAITn signal.
* These timing are specified only when HostWAITn is asserted within the cycle
* When hosts access PC Card Configuration Registers, WAITn Pulse Width is one system clock duration.
* When hosts access others, WAITn Pulse Width is dependent on system bus states
# This time is dependent on a system clock. (one system clock duration)

◆ Memory Write Timing Diagram

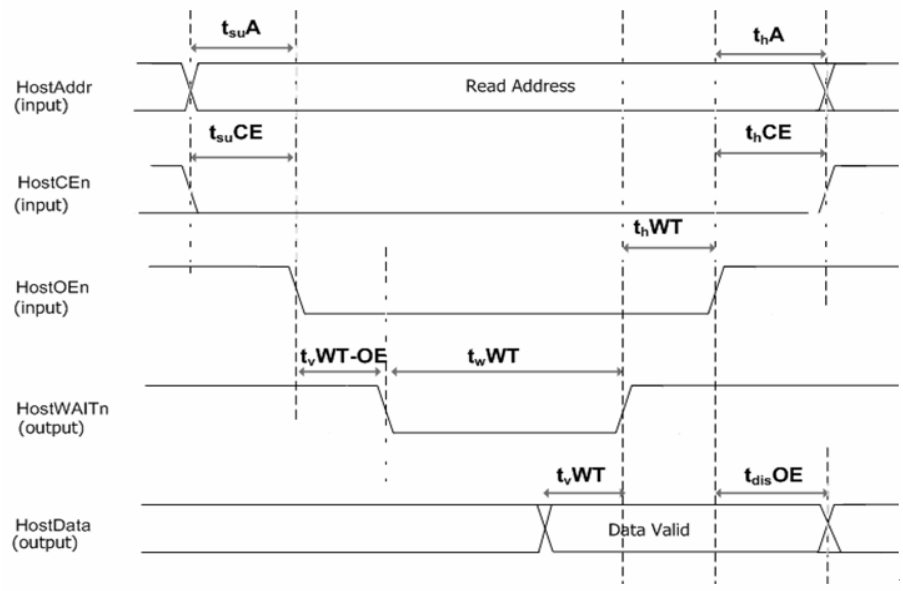


Note1. May be high or low for write timing, but restrictions on HostOEn from previous figures apply.
Note2. When data I/O pin is in the output state, no signals shall be applied to the data pins (HostData[15:0] by the host system.)
Note3. Minimum write pulse width must be met whether or not HostWaitn is asserted by card.

Speed Version			600 ns	
Item	Symbol	IEEE symbol	Min(ns)	Max(ns)
Write cycle time	t_cW	tAVAV	600	
Write Pulse Width	t_w(WE)	tWLWH	300	
Address Setup Time	t_{su}(A)	tAVWL	50	
Address Setup Time for WEn	t_{su}(A-WEH)	tAVWH	350	
Card Enable Setup Time for WEn	t_{su}(CE-WEH)	tELWH	300	
Data Setup Time for WEn	t(D-WEH)	tDVWH	150	
Data Hold Time	t_h(D)	tWMDX	70	
Write Recover Time	t_{rec}(WE)	tWMAX	70	
Output Disable Time from WEn	t_{dis}(WE)	tWLQZ		150
Output Disable Time from OEn	t_{dis}(OE)	tGHQZ		150
Output Enable Time from WEn	t_{en}(WE)	tWHQNZ	5	
Output Enable Time from OEn	t_{en}(OE)	tGLQNZ	5	
Output Enable Setup from WEn	t_{su}(OE-WE)	tGHWL	35	
Output Enable Hold from WEn	t_h(OE-WE)	tWHGL	35	
Card Enable Setup Time	t_{su}(CE)	tELWL	0	
Card Enable Hold Time	t_h(CE)	tGHEH	35	
WAITn valid from WEn	t_v(WT-WE)	tWLWTV		100
WAITn Pulse Width	t_w(WT)	tWTLWTH		12us
WEn High from WAITn Released	t_v(WT)	tWTHWH	0	

■ Host Interface (KWPAN1200)

◆ Memory Read Timing Diagram

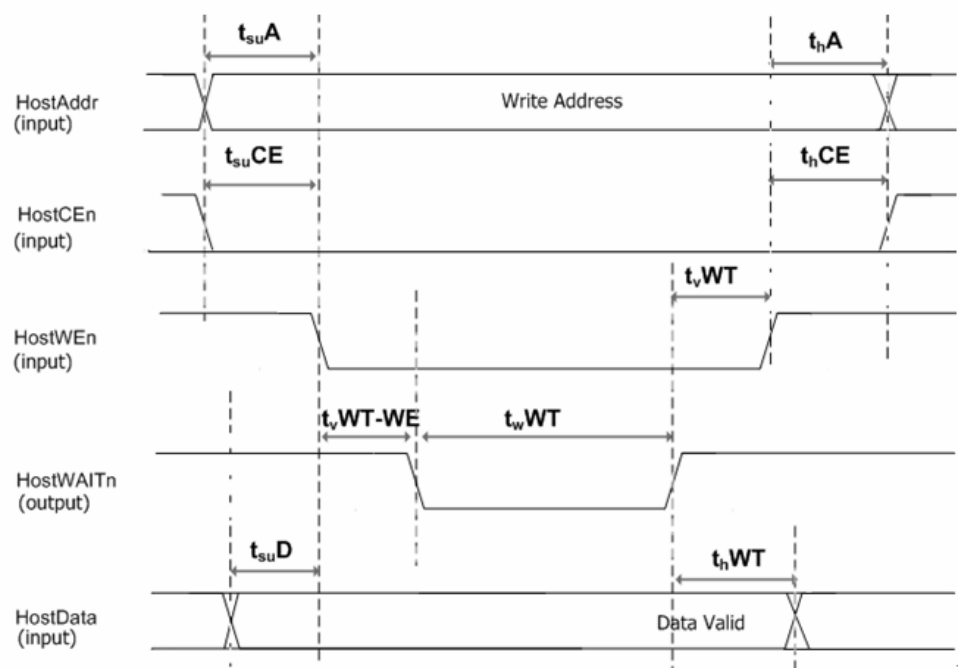


(system clock : 22MHz)

Item	Symbol	Min(ns)	Typ(ns)	Max(ns)
Output Disable Time from OEn	t_{dis}(OE)			45
Address Setup Time	t_{su}(A)	0		
Address Hold Time	t_h(A)	0		
Card Enable Setup Time	t_{su}(CE)	0		
Card Enable Hold Time	t_h(CE)	0		
OEn Valid from WAITn	t_h(WT)	0		
WAITn Valid from OEn	t_v(WT-OE)			90
WAITn Pulse Width	t_w(WT)	90		
Data Setup for WAITn Released	t_v(WT)	45		

* These timing are specified for hosts and PC card which support the HostWAITn signal.
* These timing are specified only when HostWAITn is asserted within the cycle
* When hosts access PC Card Configuration Registers, WAITn Pulse Width is one system clock duration.
* When hosts access others, WAITn Pulse Width is dependent on system bus states

◆ Memory Write Timing Diagram



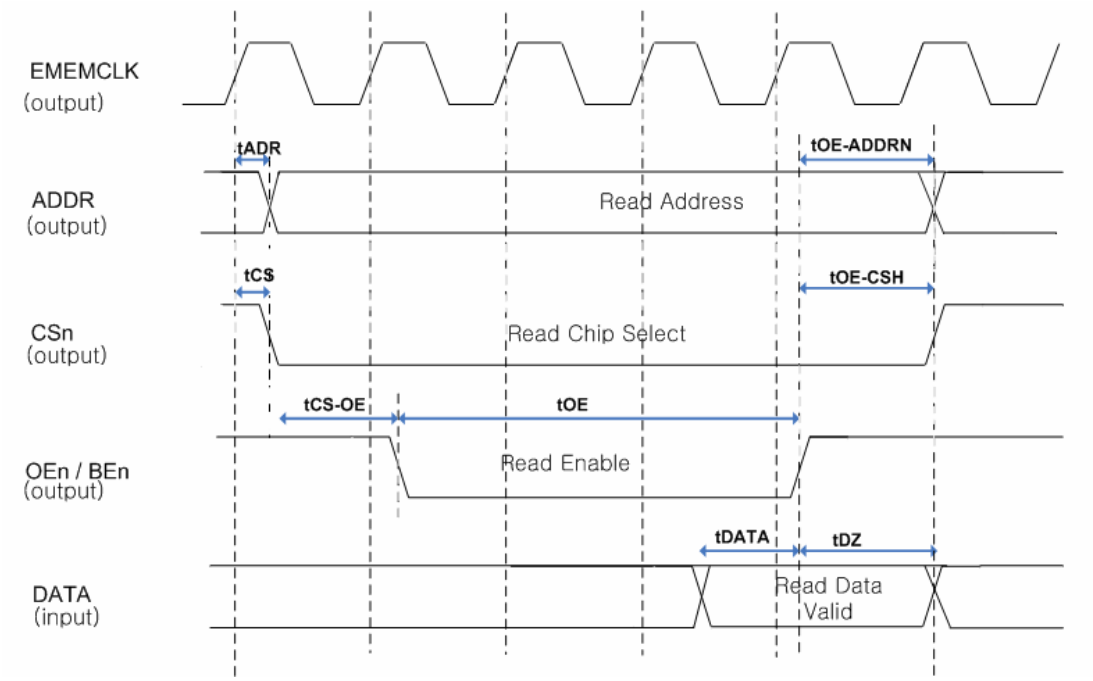
(system clock : 22MHz)

Item	Symbol	Min(ns)	Typ(ns)	Max(ns)
Address Setup Time	t_{su}(A)	0		
Card Enable Setup Time	t_{su}(CE)	0		
Data Setup Time	t_{su}(D)	0		
WAITn valid from WEn	t_v(WT-WE)			90
WAITn Pulse Width	t_w(WT)	90		
WEn High from WAITn Released	t_v(WT)	0		
Data Disable from WAITn Released	t_h(WT)	0		
Card Enable Hold Time	t_h(CE)	0		
Address Hold Time	t_h(A)	0		

* These timing are specified for hosts and PC card which support the HostWAITn signal.
* These timing are specified only when HostWAITn is asserted within the cycle
* When hosts access PC Card Configuration Registers, WAITn Pulse Width is one system clock duration.
* When hosts access others, WAITn Pulse Width is dependent on system bus states

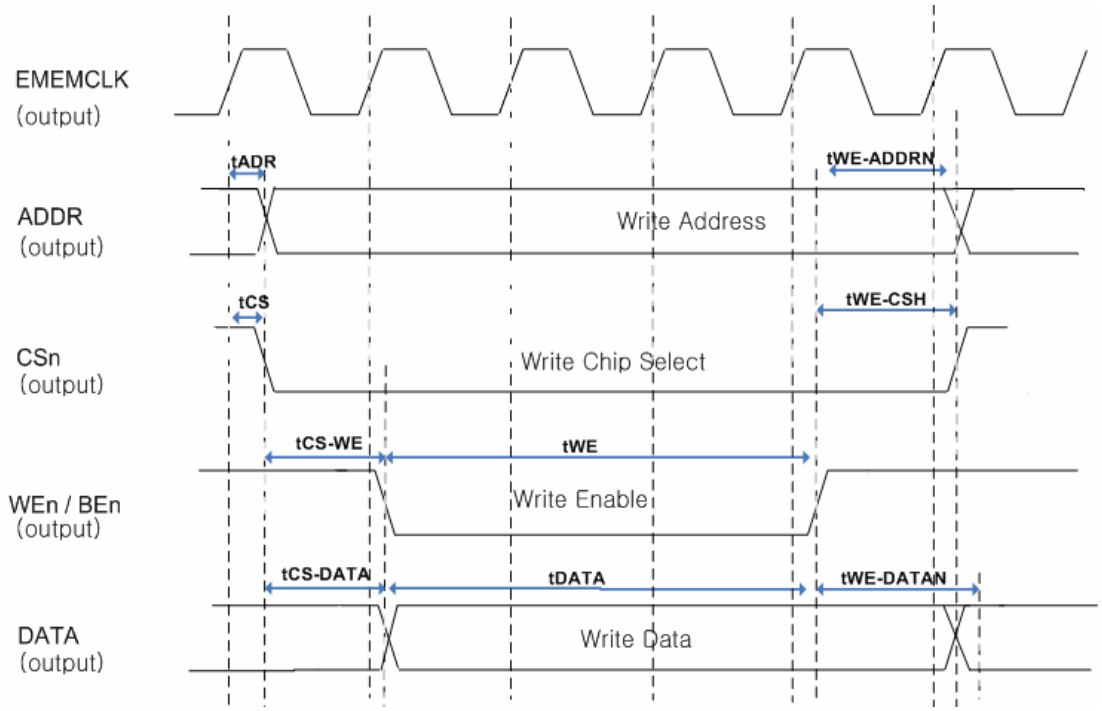
■ External Memory Interface (optional)

◆ External Memory Read Timing Diagram



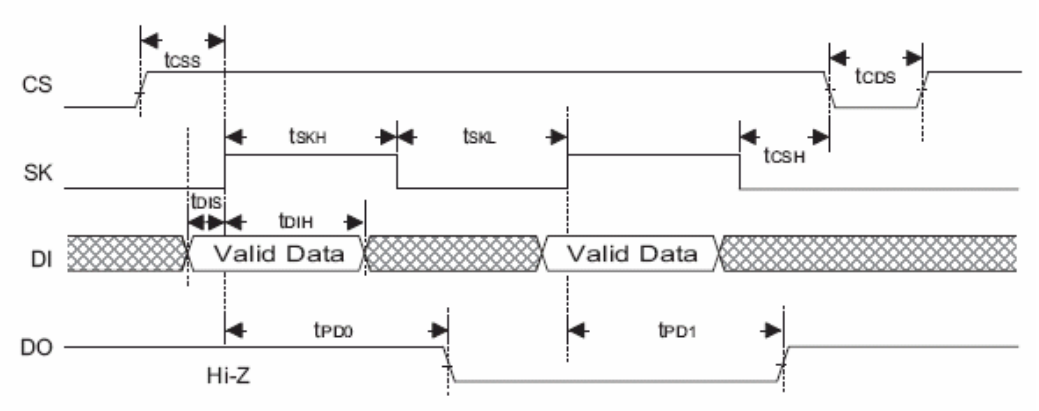
	Parameter	Min (clock)	Typ (clock)	Max (clock)
tADR	EMEMCLK rising edge to ADDR valid		0	
tCS	EMEMCLK rising edge to CSn valid		0	
tCS-OE	CSn valid to OEn/BEn valid		1	
tOE	Read Enable Pulse duration	1	TACC	15
tDATA	Read Data Valid from OEn disable		1/2	
tDZ	OEn disable to DATA invalid		1	
tDZ	OEn disable to DATA invalid		1	
tOE-CSH	OEn disable to CSn disable		1	
tOE-ADDRN	OEn disable to ADDR invalid		1	

◆ External Memory Write Timing Diagram



	Parameter	Min (clock)	Typ (clock)	Max (clock)
tADR	EMEMCLK rising edge to ADDR valid		0	
tCS	EMEMCLK rising edge to CSn valid		0	
tCS-WE	CSn enable to WEn enable		1	
tCW-DATA	CSn enable to DATA valid		1	
tWE	Write Enable Pulse duration	1	TACC	15
tDATA	Data valid duration		tWE	
tWE-CSH	WEn disable to CSn disable		1	
tWE-ADDRN	WEn disable to ADDR invalid		1	
tWE-DATAN	WEn disable to DATA invalid		1	

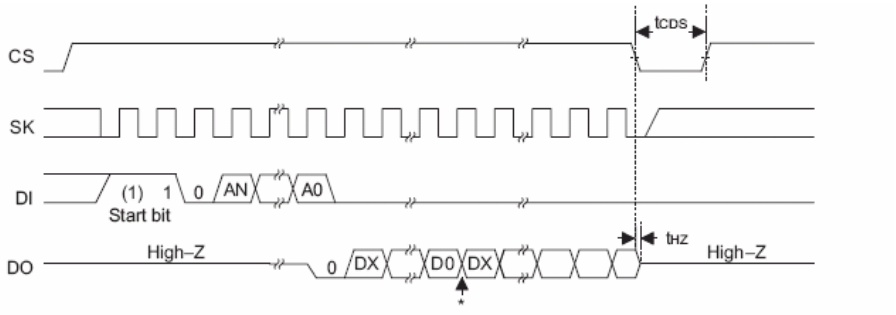
■ 3-wire Serial EEPROM Interface



A.C. Characteristics

Parameter		Min	Typ	Max	Unit
fSK	Clock frequency	0		500	KHz
tSKH	SK High Time	1000			ns
tSKL	SK Low Time	1000			ns
tCSS	CS Setup Time	200			ns
tCSH	CS Hold Time	0			ns
tCDS	CS Deselect Time	250			ns
tDIS	DI Setup Time	200			ns
tDIH	DI Hold Time	200			ns
tPD1	DO Delay to _1_			1000	ns
tPD0	DO Delay to _0_			1000	ns
tSV	Status Valid Time			250	ns
tHV	DO Disable Time	400			ns
tPR	Write Cycle Time			5	ms

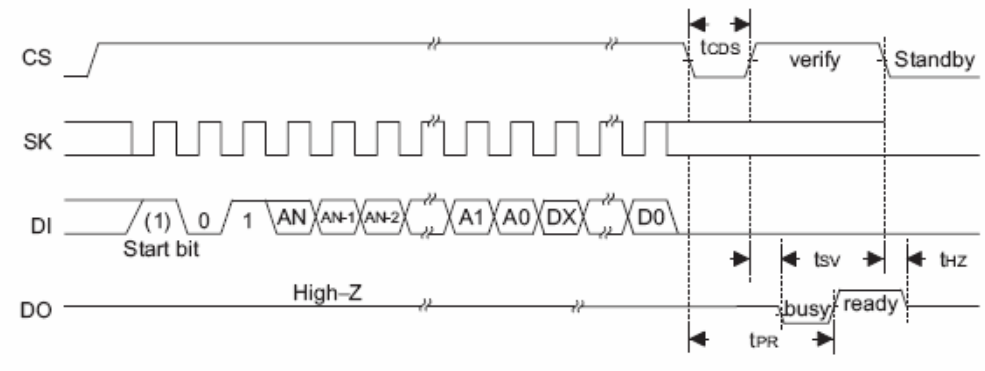
◆ Read Timing Diagram



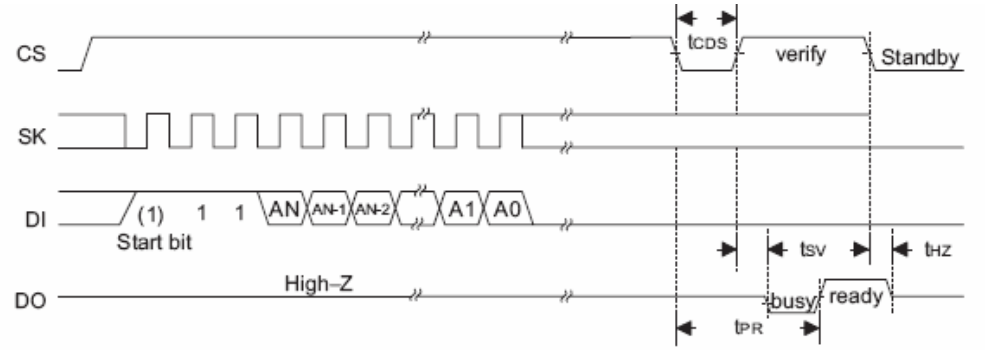
* Address pointer automatically cycles to the next word

Mode	(X16)	(X8)
AN	A5	A6
DX	D15	D7

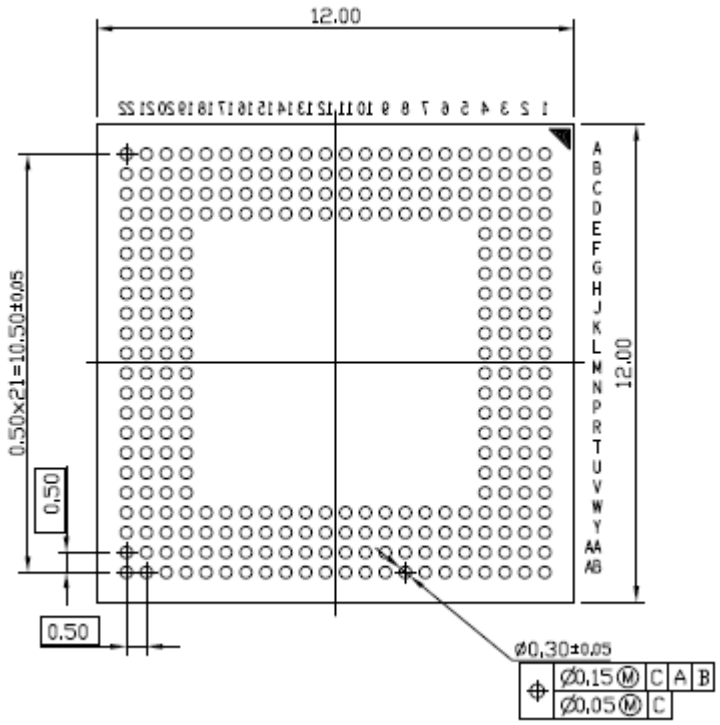
◆ Write Timing Diagram



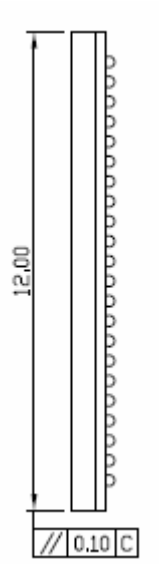
◆ Erase Timing Diagram



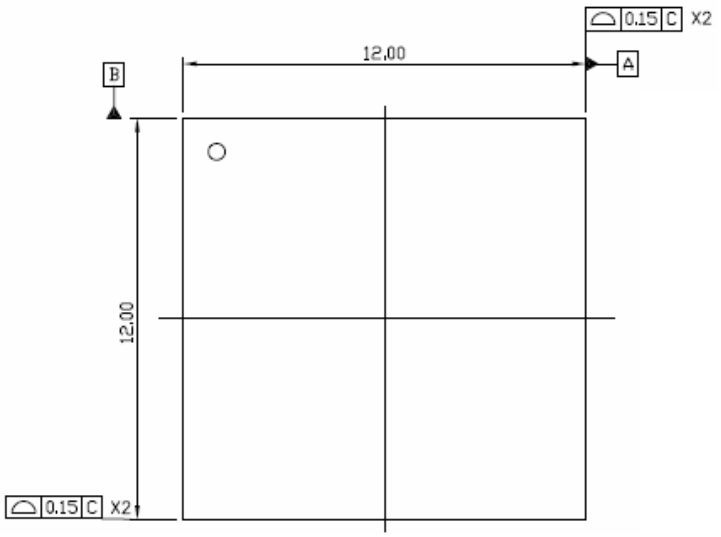
■ Package Dimension



BOTTOM VIEW



SIDE VIEW



TOP VIEW

(Unit : mm)

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